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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/760,996
Filing Date: January 20, 2004
Appellant(s): SMITH ET AL.

Charles E. Wands, Reg. No. 25,649
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 15 September 2006 appealing from the Office action mailed 18 April 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,385,336 TAKESHITA et al 5-1983

Appellant's admitted prior art, figure 1, paragraphs [02] and [03].

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 15-18, 21-24 and 27-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over appellant's admitted prior art (figure 1 and paragraphs 2 and 3) in view of Takeshita et al. (US Patent 4,385,336).**

Claim 15 is limited to "a method of delivering span power." It is noted that the appellant's admitted prior art (drawings, figure 1; and specification, paragraphs 2 and 3) describes "a method of delivering span power by way of a plurality of telecommunication wireline segments to respective ones of a plurality of remote telecommunication terminals." In particular, figure 1 depicts a central office transceiver 10 for providing

span power over "wireline" 20 to remote terminal 30. Paragraph 3 discloses a plurality of such transceivers, respective "wireline segments" and "respective remote telecommunication terminals." Paragraph 3 discloses steps (a) and (b), namely that "multiple central office transceiver units...derive span power for their respective remote transceiver units from a common...power source." The common power source corresponds to "a span power bus." While paragraph 3 of the admitted prior art identifies the ground fault problem recited in step (c), the appellant's admitted prior art fails to anticipate "coupling respective ones of said plurality of telecommunication wireline segments to respective ones of a plurality of ground fault detection and isolation circuits," and therefore, fails to anticipate steps (c), (d) and (e) and their respective substeps. As shown below, this deficiency is overcome by an obvious modification.

In particular, prior art reference Takeshita recognizes the ground fault problem in the scope of a current supplying circuit for use in a subscriber circuit (i.e. the central office transceiver of appellant's admitted prior art). See, in particular, column 1, lines 6-12, as well as the rest of column 1 and column 2, lines 1-57. In operation, the invention of Takeshita detects a ground fault in a subscriber line and reduces current thereto (i.e. "isolates"). See column 2, lines 30-54, as well as column 3, lines 44-52. The invention of Takeshita is generally applicable to any and all current supplying circuits disclosed by appellant's admitted prior art, and thus meets step (c), which is directed toward providing ground fault detection and isolation for each wireline segment. Simply providing the ground fault circuits of Takeshita as taught will enable them to detect and isolate circuits as recited in step (d). Isolation in response to ground fault detection

occurs in accordance with step (e). See column 3, lines 44-52. Steps (d1) and (d2) were shown to be taught by Takeshita apropos the rejection of claim 1 in the Non-Final Rejection filed 25 August 2005.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to add the functionality for detecting and isolating ground faults as taught by Takeshita for the purpose of removing ground faults that can be potentially dangerous. See Takeshita column 1, lines 6-12; and appellant's specification, paragraph 3, lines 5-16.

Claims 16-18 are limited to "the method according to claim 15," as covered by appellant's admitted prior art in view of Takeshita. First, note that claims 16-18 define essentially the same subcombination (i.e. ground fault detection and isolation) as originally filed claims 2-4. The rejections of claims 2-4 are reproduced herein below and matched to claims 16-18 for convenience.

Claim 16 is limited to "the method according to claim 15," as covered by appellant's admitted prior art in view of Takeshita. Takeshita discloses a current supplying circuit with a shorted-to-ground fault detecting function. See Abstract. Generally depicted in figure 1, the current supplying circuit includes a battery (6) for supplying current on feed line (1) and a return for current upon feed line (2). Two resistor circuits (3) and (4) are connected in series with the feed lines, the current through the resistors detected by current detectors (8) and (9), respectively, and the detected currents through each resistor are compared by comparator (10) to detect a ground fault. See column 3, line 24, through column 4, line 8. With respect to the claim

as recited, the current detector (8) and the current detector (9) perform functions corresponding to measuring first and second parameters representative of current flowing through a first and second portion of a wireline, respectively. The comparator (10) detects a difference between these parameters and provides an output indicating a ground fault.

Figure 3 depicts a more detailed view of one embodiment of figure 1. In particular, each of the resistors (3) and (4) comprise a resistor in series with the feed paths seen in figure 3. The resistors correspond to the recited first and second sense resistors. The recited first and second voltages correspond to either the voltages presented at nodes a and b of the differential amplifier (10) or the voltages across the base and emitter of transistors Q_6 and Q_7 or a combination thereof. In any case, the voltages are compared to each other due to the common emitter configuration of the differential amplifier (10). In response, an output SCN is generated, signaling the absence or presence of a ground fault. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

Claim 17 is limited to "the method according to claim 16," as covered by appellant's admitted prior art in view of Takeshita. Still referring to figure 3, the sense resistor (3) is coupled to detector (8), which essentially mirrors a representative current through resistor R_{1A} to node "a." The current generated through circuit (8) is coupled to the differential amplifier (10). The amplifier allows output current to flow through resistors R_{12}; the current through the resistor leaks through the base to node "a" and through the collector to resistors R_9 and R_8. The base current combines with the mirror

current to form the first voltage across resistor R_{11}. The collector current controls the current through transistor Q_8, which corresponds to a controlled current device. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

Claim 18 is limited to "the method according to claim 17," as covered by appellant's admitted prior art in view of Takeshita. As seen in figure 3, the voltage across resistor R_{1B} is coupled to the inputs of a differential amplifier formed at least in part by the transistors Q_{12B}, Q_{13B}, Q_{1B} and Q_{0B}. The output voltage across resistor R_{0B} is passed to the base node "b" as the second voltage and is differentially combined with the voltage at node "a," which corresponds to the first voltage. Their difference indicates the presence or absence of a ground fault. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

Claim 21 is limited to "a method of delivering power." As shown in the rejection of claim 16, appellant's admitted prior art sets forth a method of providing power from a common supply source to a plurality of remote terminals by way of a plurality of respective wireline segments and respective central office transceivers. Further, it would have been obvious to provide ground fault detection and isolation as taught by Takeshita. Steps (a)-(e), (d1) and (d2) are essentially the same as the corresponding steps in claim 16. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

Claims 22-24 are limited to "the method according to claim 21," as covered by appellant's admitted prior art in view of Takeshita. First, note that claims 22-24 define

essentially the same subcombination (i.e. ground fault detection and isolation) as originally filed claims 2-4. The rejections of claims 22-24 are essentially the same as those of claims 16-18 above, and are omitted for the sake of brevity. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

Claim 27 is limited to "a system for controlling deliver of span power." The system of claim 27 necessarily follows from executing either methods defined in claims 15 or 21. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

Claim 28 is limited to "the system according to claim 27," as covered by appellant's admitted prior art in view of Takeshita. The system defined herein necessarily follows from the methods of either claim 16 or 22. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

Claim 28 is limited to "the system according to claim 27," as covered by appellant's admitted prior art in view of Takeshita. The system defined herein necessarily follows from the methods of either claims 17 and 18 or 23 and 24. Therefore, appellant's admitted prior art in view of Takeshita makes obvious all limitations of the claim.

(10) Response to Argument

Review of evidence relied upon.

Starting at the bottom of page 15 through page 18, line 9, appellant alleges that paragraph [02] is the only section of appellant's specification that describes what was known in the prior art. Namely, that it was known to provide a single pair of transceivers between a central office and a remote site linked by a twister pair 20. Appellant goes on to say that the use of multiple central office transceivers connected to a common power source is actually part of the appellant's invention. See page 16, lines 5-9, as well as page 17, lines 12-13. The chief problems with appellant's contention are that: (1) the use of multiple transceivers is indicated in the "Background of the Invention," and not introduced in the summary or detailed description of the invention; (2) the appellant does not include a figure of multiple transceivers merely connected to a common span power bus, but rather multiple transceivers connected with ground fault detect circuits, which obviate the problems discussed in paragraph [03]; (3) appellant uses language in paragraph [03] to indicate that providing multiple transceivers to a common span powered bus was well-known, e.g. *"it is often desirable for multiple central office transceiver units to derive span power for their respective remote transceiver units from a common or shared electrical power source;"* (4) appellant discloses in paragraph [05] of the specification that, *"the present invention is directed to a methodology and subsystem architecture for detecting the occurrence of a ground fault in a multiple, span-powered telecommunication network,"* which presupposes such a network. Granting (4)—that the appellant actually invented the multiple, span-powered telecommunication network—begs the question: where is the supporting disclosure? It

is not surprising that appellant did not actually invent coupling multiple transceivers to a common power bus since the original claims were directed solely toward the subcombination, i.e. the ground fault detector for use in such an environment. The shift in focus to the combination being permissible only in view of the fact that the now claimed combination includes all limitations of the originally presented subcombination, which is what the appellant's invention truly is.

Within pages 15-18, appellant further alleges that only appellant recognizes the ground fault problem, and that the section of paragraph [03] explaining the ground fault problem is solely the pontification of the appellant. However, as shown above, the appellant is mistaken in alleging that paragraph [03] is his own. The above notwithstanding, appellant's allegation is rendered moot by Takeshita's identification of the ground fault problem in current supplying circuits in a subscriber circuit, which corresponds to a central office transceiver. It is true, that Takeshita may not recognize that ground faults on one subscriber line will effect other subscriber lines since there is no disclosure of a common power bus, but Takeshita does motivate the use of a ground fault detector for other reasons, like protection against damage. See column 1, lines 6-12. In this way, it is clear that knowledge of ground faults was known at the time of the invention.

The rejections of claims 15-18, 21-24 and 27-29 under 35 U.S.C. 103(a) as being unpatentable over appellant's admitted prior art in view of Takeshita et al. (US Patent 4,385,336).

Herein below, all efforts were made to address each and every allegation made by the appellant. Any discontinuity between cited line numbers lies is a result only of a decision that appellant's arguments were already completely treated and including further argument would render this answer overly redundant.

On page 20, lines 1-14, appellant alleges that the examiner erred in using paragraph [03] as admitted prior art. This point was shown under the preceding heading to be mistaken. Not only is paragraph [03] prior art, but Takeshita also describes that supplying current remotely inherently risks a ground fault. It does not matter how many central office transceivers are present, ground fault is possible on all subscriber lines.

Understanding the rejection, appellant's prior art at a minimum discloses multiple central office transceivers, each coupled to a common power bus. Takeshita, at least, recognizes that ground fault may occur on a subscriber line connected to a transceiver. In solution, Takeshita places **a** ground fault detection and removal circuit in **a** subscriber circuit for **a** subscriber terminal. Since appellant's prior art has multiple subscriber circuits and terminals, a ground fault detection circuit obviously must be provided in each to obviate ground fault for each one, a concept that cannot be any more elementary.

On page 21, lines 18-19, the appellant appears to suggest that the multiple segment span-powered system is prior art. **Clarification for the record of the appellant's stance should be provided in a Reply Brief.** This confusion on the part of the appellant undergirds the examiner's position that upon reading appellant's

specification, one of ordinary skill in the art would immediately recognize the "Background of the Invention" as admitted prior art.

On page 21, line 29, through page 22, line 2, appellant suggests a misunderstanding of the phrase "Takeshita recognizes the ground fault problem 'in the scope of' a current supplying circuit for use in a subscriber circuit." Recognizing the idiosyncratic nature of the term, it is noted that "in the scope of" means "in the field of." In other words, Takeshita's disclosure is directed towards ground faults in a current supplying circuit for use in a subscriber circuit.

On page 22, lines 3-15, appellant alleges that the invention of claim 21 does not reside in the central office. In particular, claim 21 recites, "coupling first and second portions of respective ones of said plurality of telecommunication wireline segments to respective ones of a plurality of ground fault detection and isolation circuits." So, a first and second "portion" of a wireline segment are connected to a ground fault circuit. This is plain, broad language meaning that any two parts of the wireline are connected to a ground fault circuit. This is shown in figure 1 of Takeshita, where portions 1 and 2 of a wireline are connected to a ground fault circuit by way of transformer 5.

Moreover, appellant's sole figure depicting the spatial relationship between the ground fault detectors and the wirelines is figure 3, which shows the ground fault detector in the DSL-C (Digital Subscriber Line—Central Office Terminal).

On page 22, lines 16-26, appellant alleges that the ground fault-based control mechanism employed by the circuit of Takeshita is installed in a subscriber circuit, such as a telephone handset. In support of this allegation, the appellant refers to column 3,

lines 3-5 of Takeshita: "a subscriber terminal such as a telephone set being connected through the tip and ring lines to the terminals 1 and 2." However, column 1, lines 6-9, recite: "the present invention relates to current supplying circuits for use in a subscriber circuit," i.e. not in a terminal but the notoriously well-known subscriber line interface circuit (SLIC), "for supplying speech signals to a subscriber terminal, in a telephone exchange or the like." This makes it clear that the subscriber circuit is in a telephone exchange, i.e. central office. Column 3, lines 5-8 does not say that the subscriber circuit is in a terminal either.

On page 22, line 27, through page 24, line 21, appellant alleges that the circuit of Takeshita is for the purpose of "controlling the internal resistance" of the speech current supplying circuit of a telephone handset and not for isolating a span-powered telecommunication wirelines segment. Considering that the appellant fails in his specification to define isolation, a reasonable ordinary and plain meaning has been assigned in rejecting the claims. In particular, isolation in the field of electronics refers to eliminating the influence of an electrical current on another current. In the case of Takeshita, increasing resistance R causes a corresponding linear decrease in current flow I as defined by Ohm's Law ($V = I * R$ or $I = V / R$). If resistance is increased far enough, galvanic isolation is provided. Moreover, the appellant has provided absolutely no reason to believe reducing current consumption is not the same as isolation in any of pages 22-24.

On page 24, line 22, through page 25, line 13, appellant alleges that the examiner's position that the teachings of Takeshita are generally applicable to all

current providers is unsupported. However, figure 1 of Takeshita is incredibly generalized, depicting only a battery as a current provider. A battery is as basic as power supplies get. The appellant continues on page 25 to indicate that Takeshita only controls the internal resistance, and does not isolate the battery 6 from lines 1 and 2. However, increasing the resistance decreases the current. In fact, as the resistance approaches infinity, an "open-circuit" is defined. In other words, an "open-circuit" occurs when no current passes through two nodes. One simple example is a switch. If the switch is closed current passes, if it is open no current passes. Under the appellant's logic, simulating an "open-circuit," as does Takeshita, does not provide isolation, which is simply absurd.

On page 25, lines 14-30, appellant alleges that Takeshita does not teach providing ground fault circuits in respective wireline segments. This is true to an extent since Takeshita focuses on a single instance of a current supplying subscriber circuit. However, increasing the number of subscriber circuits as done in appellant's admitted prior art creates more instances for ground fault to occur. The only way to solve all possible occurrences of ground fault in view of Takeshita is to provide the ground fault protector of Takeshita in all subscriber circuits.

On page 25, last line, through page 26, line 11, appellant continues to allege that Takeshita does not isolate, but only increases resistance. This argument has been treated thoroughly supra.

On page 27, lines 16-30, appellant again tries to recast the admitted prior art as that which he invented. As shown above, appellant admitted a multiple transceiver unit

architecture. As pointed out above, paragraph [03] includes suggestive language indicating prior knowledge, the remainder of the specification is directed towards detecting ground faults (not even how to isolate), etc...Moreover, Takeshita recognizes that ground faults occur in any remote current supply arrangement involving subscriber wirelines. Although Takeshita does not expressly teach providing a detector in multiple central office transceivers, it is clear from reading Takeshita that ground faults would occur in every instance pair of a central office transceiver and subscriber wireline, requiring a ground fault detector as taught by Takeshita in each instance.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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